amd fnl 1 dnf   4   2/28/2006 11:26 AM

Please amend the claims as follows:

1. (Currently Amended)   A method of operating a memory management system
5   for processing data files <u>received by a file server</u>, said system comprising an
       access flow regulator, a plurality of high speed low storage capacity memories and
       a lower speed high storage capacity bulk memory, said high speed memories have
       a first data rate, said bulk memory has a second data rate substantially lower than
       said first data rate; <u>said access flow regulator being adapted to generate requests</u>
10   <u>received from said file server for the reading and writing of data files by said</u>
       <u>memories, said access flow regulator defines and interface between said file server</u>
       <u>and said memory management system</u>, said method comprises the steps of:
              operating said access flow regulator for generating requests for the reading
       and writing of said memories;
15   initiating the writing of a data file by transmitting a write request from said
       access flow regulator to one of said high speed memories, said data file has a first
       portion and an excess portion;
              writing said first part and said excess portion of said data file into said one
       high speed memory; and
20   transferring said excess portion of said data file from said one high speed
       memory to said bulk memory while leaving said first portion of said data file in said
       one high speed memory.

2. (Currently Amended)   A method of operating a memory management system
25   <s>for processing</s> <u>adapted to store</u> data files <u>received by a file server</u>, said system
       comprising an access flow regulator, a plurality of high speed low storage capacity
       memories and a lower speed high storage capacity bulk memory, said high speed
       memories have a first data rate, said bulk memory has a second data rate
       substantially lower than said first data rate, <u>said system comprising an access flow</u>
30   <u>regulator adapted to generate requests received from said file server for the</u>
       <u>reading and writing of data files by said memories, said access flow regulator</u>
       <u>defines and interface between said file server and said memory management</u>
       <u>system</u>, said method comprises the steps of:
              operating said access flow regulator for generating requests for the reading
35   and writing of said memories;

amd fnl 1 dnf   5   2/28/2006 11:26 AM

initiating the reading of a data file by transmitting a ~~write~~ <u>read</u> request from said access flow regulator to one of said high speed memories, said data file has a first portion and an excess portion;

transmitting a read request for a data file from said access flow regulator to a

5   one high speed memory storing a first part of said data file;

reading said first portion of said data file from said one high speed memory;

transferring said excess portion of said data file from said bulk memory to said one high speed memory;

reading out said excess portion of said data file from said one high speed

10   memory; and

transmitting said first part and said excess portion said data file to said access flow regulator.

3. (Currently Amended)   The method of claim 1 further including the step of

15   operating said system to concurrently ~~processes~~ <u>process</u> data files for a plurality of requests from said access flow regulator.

4. (Original)   The method of claim 1 further including the step of operating said system to concurrently process a plurality of data files stored in different ones of

20   said high speed memories.

5. (Original)   The method of claim 1 wherein said system further comprises a plurality of state controllers each of which is individual to one of said high speed memories, said system further comprises an access bus connecting said access

25   flow regulator with said state controllers, said step of transmitting a write request includes the steps of:

operating said access flow regulator to select an idle high speed memory that is to receive said write request;

transmitting said write request from said access flow regulator over said

30   request bus to the state controller individual to said selected high speed memory; and

operating said state controller to extend said write request to the high speed memory.

amd fnl 1 dnf   6   2/28/2006 11:26 AM

6. (Original) The method of claim 5 wherein said step of operating said state controller to transmit said write request includes the steps of:

    determining the present occupancy level of said selected high speed memory;

5   transmitting said request to said selected high speed memory if said present occupancy is not exceeded; and

    requesting a signalwise connection of said access flow regulator to said bulk memory if said present occupancy level of said selected high speed memory is exceeded.

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7. (Original) The method of claim 5 wherein said system further includes a multiplexer, and an access bus connecting said state controllers with said multiplexer, and said system further includes a bus connecting said multiplexer with said bulk memory, said method includes the further steps of:

15   transmitting a request to said multiplexer for the transfer of data files from said state controllers to said bulk memory;

    determining which one of a plurality of requesting state controllers is to be granted access to said bulk memory;

    connecting signalwise said one requesting state controller to said bulk

20   memory; and

    controlling the operation of said bulk memory in the transfer of data from said selected high speed memory to said bulk memory.

8. (Original) The method of claim 7 including the further step of applying said data

25   file from said high speed memory and said state controller via said multiplexer and said bus to said bulk memory.

9. (Original) The method of claim 2 wherein said step of transferring said data file from said bulk memory includes the steps of:

30   reading out files from said bulk memory to said high speed memories in a burst mode at a data rate substantially equal to the data rate of said high speed memories;

    storing said read out files in said high speed memories; and

amd fnl 1 dnf   7   2/28/2006 11:26 AM

reading out said data file from said high speed memory for transfer to said access flow regulator.

10. (Currently Amended)   The method of claim 5 wherein said step of operating said state controllers to transmit said write request includes the further steps of:

concurrently serving multiple write requests directed to multiple files;

serving the multiple write file requests received by said access flow regulator; and

extending multiple write requests received by said access flow regulator to said high speed memories.

11. (Original) The method of claim 5 wherein said step of operating said state controller includes the further steps of:

processing each received request to determine the present occupancy level of said high speed memory;

extending said request to said high speed memories if said present occupancy level is not exceeded; and

buffering said request in said access flow regulator if said present occupancy level is exceeded.

12. (Original) The method of claim 5 wherein said step of operating said state controllers includes the further steps of:

controlling the transfer of a data file from said high speed memory to said bulk memory; and

controlling the transfer of a data file from said bulk memory to said high speed memories.

13. (Original)   The method of claim 5 wherein said step of operating said state controllers includes the further steps of:

determining whether said bulk memory is idle when a transfer is requested;

extending said data file to said bulk memory if said bulk memory idle; and

buffering said transfer request if said bulk memory is busy.

amd fnl 1 dnf   8   2/28/2006 11:26 AM

14. (Original)   The method of claim 7 wherein said step of operating said multiplexer includes the further steps of:

determining which one of a plurality of requesting high speed memories is to be granted access to said bulk memory;

5   granting the request to one of said high speed memories; and

buffering the requests of all but said one high speed memories.

15. (Original)   The method of claim 7 wherein said step of operating said multiplexer includes the further steps of:

10   determining the identity to the one of said high speed memories to which a data file is to be directed by said multiplexer; and

controlling the transfer of said data file from said bulk memory to said identified high speed memory.

15   16. ((Currently Amended)   A method of operating the memory management system of claim 1, said method comprising the further steps of:

generating a signal unique to each said high speed memory indicating the busy / idle state of each said high speed memory;

extending each generated busy / idle signal to said access flow regulator;

20   operating said access flow regulator to receive requests for the writing or reading of files by said memories;

operating said access flow regulator in response to the receipt of said request to read said busy / idle signals;

· operating said access flow regulator in response to said reading to identify

25   an idle one of said memories; and

operating said access flow regulator for extending a request for the reading and writing of a data file to said idle one high speed memory.

17. (Currently Amended)   A memory management system defining a file server

30   adapted to process received data files, said system comprises:

a plurality of low storage capacity high speed memories and a lower speed high storage capacity bulk memory, said high speed memories have a first data rate and said bulk memory has a second data rate lower than said first data rate;

amd fnl 1 dnf   9   2/28/2006 11:26 AM

an access flow regulator for generating requests for the reading and writing
of files by said memories; said access flow regulator being adapted to generate
requests received from said file server for the reading and writing of data files by
said memories, said access flow regulator defines an interface between said file
5   server and said memory management system ,

apparatus for operating said access flow regulator to initiate the writing of a
data file stored in said memories by transmitting an access ~~read~~ write request to the
one of said high speed memories;

apparatus for writing a first part and excess part of said data file into said
10   one high speed memory;

apparatus for transferring said excess part of said data file from said one
high speed memory to said bulk memory while leaving the first part of said data file
in said one high speed memory;

apparatus for subsequently transmitting a read request for said data file from
15   said access flow regulator to said one high speed memory;

apparatus for reading said first part in said one high speed memory;

apparatus for transferring said excess part of said data file from said bulk
memory to said one high speed memory;

apparatus for reading out said first part and said excess part of said data file
20   from said high speed memory; and

apparatus for transmitting said read out data file to said access flow
regulator.

18. (Currently Amended)   The system of claim 17 further comprising:
25   apparatus for generating a signal unique to each high speed memory
indicating the busy / idle state of each said high speed memory;

apparatus for extending each generated busy / idle said signal to said
access flow regulator;

apparatus for operating said access flow regulator to receive a request for
30   the writing or reading of data files by said memories;

apparatus for operating said access flow regulator in response to the receipt
of said request to read each said busy / idle signal;

apparatus for operating said access flow regulator in response to said
reading to determine the current busy / idle state of each of said memories; and

amd fnl 1 dnf   10   2/28/2006 11:26 AM

apparatus for operating said access flow regulator in response to a
determination that one of said memories is currently idle for granting a request for
the reading or writing of a data file by said one memory.